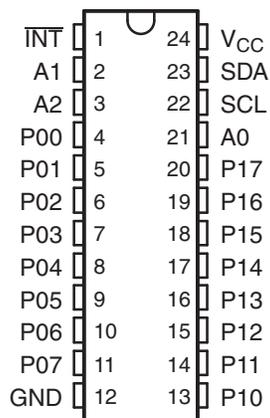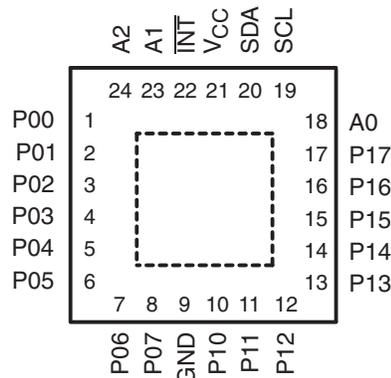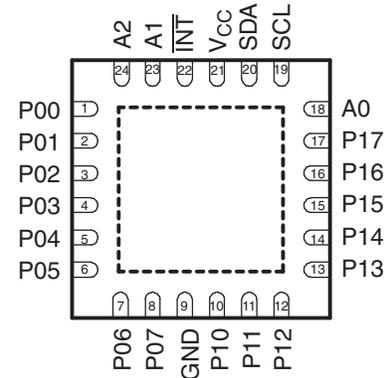# Ti TEXAS INSTRUMENTS

REMOTE 16-BIT I^{2}C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS

FEATURES

- **Low Standby-Current Consumption of 1 μA Max**
- **I^{2}C to Parallel Port Expander**
- **Open-Drain Active-Low Interrupt Output**
- **5-V Tolerant I/O Ports**
- **Compatible With Most Microcontrollers**
- **400-kHz Fast I^{2}C Bus**
- **Address by Three Hardware Address Pins for Use of up to Eight Devices**

- **Polarity Inversion Register**
- **Latched Outputs With High-Current Drive Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)

INT	1	24	V$_{CC}$
A1	2	23	SDA
A2	3	22	SCL
P00	4	21	A0
P01	5	20	P17
P02	6	19	P16
P03	7	18	P15
P04	8	17	P14
P05	9	16	P13
P06	10	15	P12
P07	11	14	P11
GND	12	13	P10

RGE PACKAGE (TOP VIEW)

Top pins: A2 (24), A1 (23), INT (22), V$_{CC}$ (21), SDA (20), SCL (19)

P00	1	18	A0
P01	2	17	P17
P02	3	16	P16
P03	4	15	P15
P04	5	14	P14
P05	6	13	P13

Bottom pins: P06 (7), P07 (8), GND (9), P10 (10), P11 (11), P12 (12)

RTW PACKAGE (TOP VIEW)

Top pins: A2 (24), A1 (23), INT (22), V$_{CC}$ (21), SDA (20), SCL (19)

P00	1	18	A0
P01	2	17	P17
P02	3	16	P16
P03	4	15	P15
P04	5	14	P14
P05	6	13	P13

Bottom pins: P06 (7), P07 (8), GND (9), P10 (10), P11 (11), P12 (12)

DESCRIPTION/ORDERING INFORMATION

This 16-bit I/O expander for the two-line bidirectional bus (I^{2}C) is designed for 2.3-V to 5.5-V V$_{CC}$ operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^{2}C interface [serial clock (SCL), serial data (SDA)].

The PCA9535 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the PCA9535 in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I^{2}C/SMBus state machine.

The PCA9535 open-drain interrupt (INT) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

INT can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^{2}C bus. Thus, the PCA9535 can remain a simple slave device.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PCA9535

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption.

Although pin-to-pin and I^{2}C address compatible with the PCF8575, software changes are required due to the enhancements.

The PCA9535 is identical to the PCA9555, except for the removal of the internal I/O pullup resistor, which greatly reduces power consumption when the I/Os are held low.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^{2}C address and allow up to eight devices to share the same I^{2}C bus or SMBus. The fixed I^{2}C address of the PCA9535 is the same as the PCA9555, PCF8575, PCF8575C, and PCF8574, allowing up to eight of these devices in any combination to share the same I^{2}C bus or SMBus.

ORDERING INFORMATION

| T$_A$	PACKAGE[1][2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DB	Reel of 2000	PCA9535DBR	PD9535
		Tube of 60	PCA9535DB	
	QSOP – DBQ	Reel of 2500	PCA9535DBQR	PCA9535
	TVSOP – DGV	Reel of 2000	PCA9535DGVR	PD9535
	SOIC – DW	Tube of 25	PCA9535DW	PCA9535
		Reel of 2000	PCA9535DWR	
	TSSOP – PW	Tube of 60	PCA9535PW	PD9535
		Reel of 2000	PCA9535PWR	
	QFN – RGE	Reel of 3000	PCA9535RGER	PD9535
	QFN – RTW	Reel of 3000	PCA9535RTWR	PD535

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

TERMINAL FUNCTIONS

NO.		NAME	DESCRIPTION
SOIC (D), SSOP (DB), QSOP (DBQ), TSSOP (PW), AND TVSOP (DGV)	QFN (RGE AND RTW)		
1	22	$\overline{\text{INT}}$	Interrupt output. Connect to V_{CC} through a pullup resistor.
2	23	A1	Address input. Connect directly to V_{CC} or ground.
3	24	A2	Address input. Connect directly to V_{CC} or ground.
4	1	P00	P-port input/output. Push-pull design structure.
5	2	P01	P-port input/output. Push-pull design structure.
6	3	P02	P-port input/output. Push-pull design structure.
7	4	P03	P-port input/output. Push-pull design structure.
8	5	P04	P-port input/output. Push-pull design structure.
9	6	P05	P-port input/output. Push-pull design structure.
10	7	P06	P-port input/output. Push-pull design structure.
11	8	P07	P-port input/output. Push-pull design structure.
12	9	GND	Ground
13	10	P10	P-port input/output. Push-pull design structure.
14	11	P11	P-port input/output. Push-pull design structure.
15	12	P12	P-port input/output. Push-pull design structure.
16	13	P13	P-port input/output. Push-pull design structure.
17	14	P14	P-port input/output. Push-pull design structure.
18	15	P15	P-port input/output. Push-pull design structure.
19	16	P16	P-port input/output. Push-pull design structure.
20	17	P17	P-port input/output. Push-pull design structure.
21	18	A0	Address input. Connect directly to V_{CC} or ground.
22	19	SCL	Serial clock bus. Connect to V_{CC} through a pullup resistor.
23	20	SDA	Serial data bus. Connect to V_{CC} through a pullup resistor.
24	21	V_{CC}	Supply voltage

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Product Folder Link(s): *PCA9535*

LOGIC DIAGRAM (POSITIVE LOGIC)
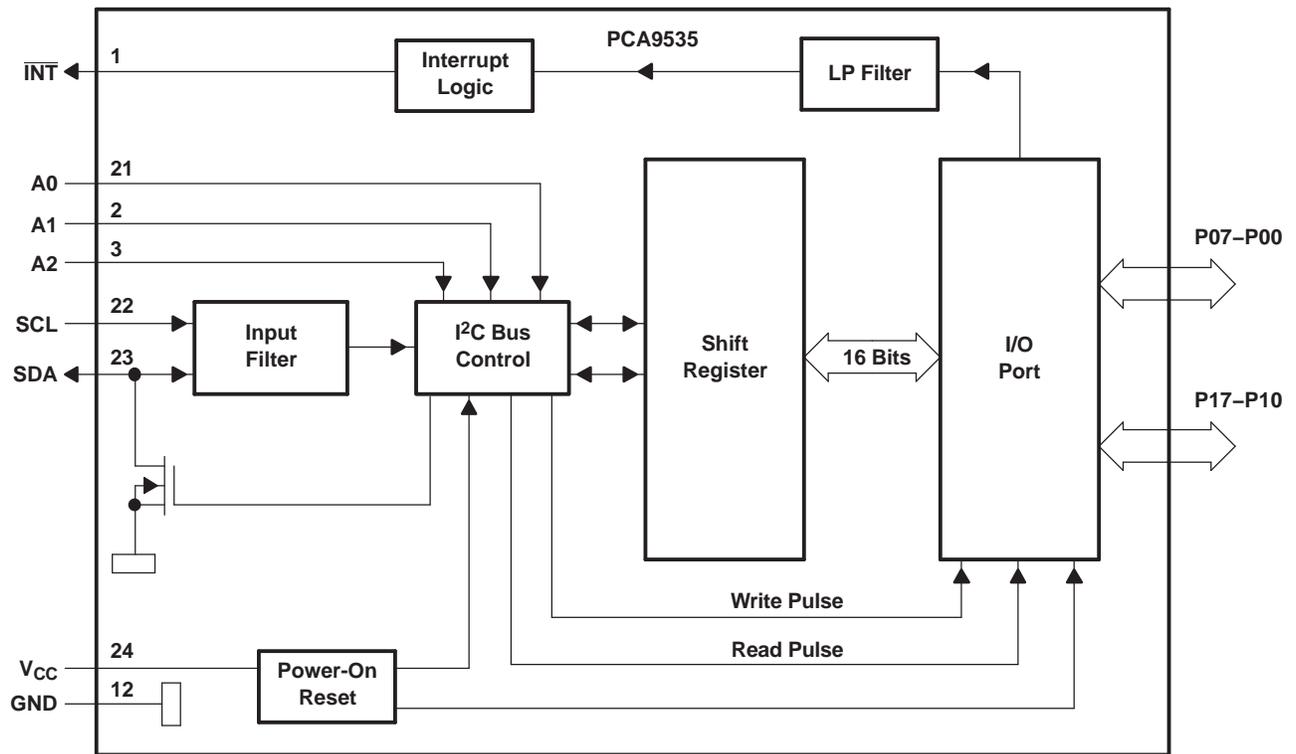
A. Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.

B. All I/Os are set to inputs at reset.

Product Folder Link(s): *PCA9535*

SIMPLIFIED SCHEMATIC OF P-PORT I/Os[1]
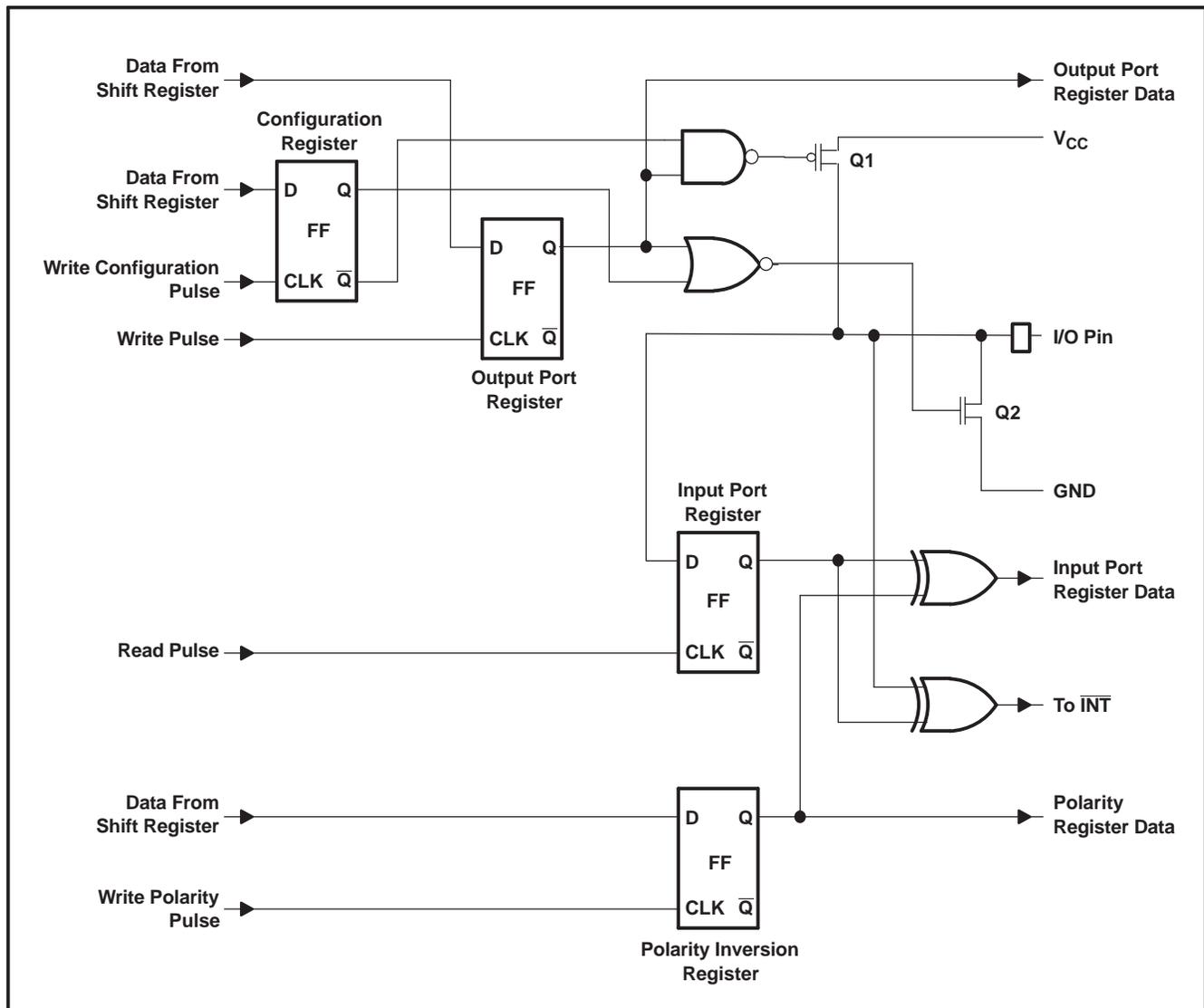
(1)   At power-on reset, all registers return to default values.

I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

I^{2}C Interface

The bidirectional I^{2}C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^{2}C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address.

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and Stop conditions.

On the I^{2}C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 2).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.
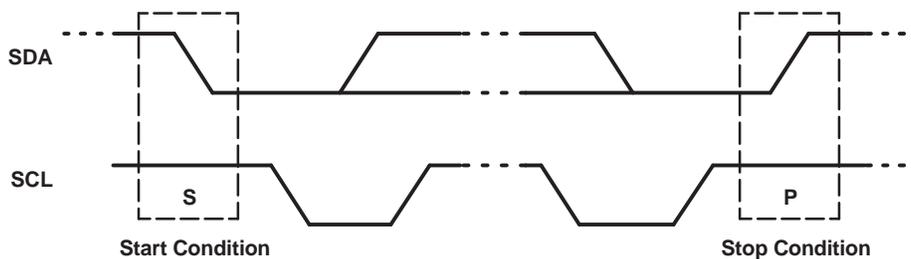
Figure 1. Definition of Start and Stop Conditions

Figure 2. Bit Transfer

Product Folder Link(s): *PCA9535*
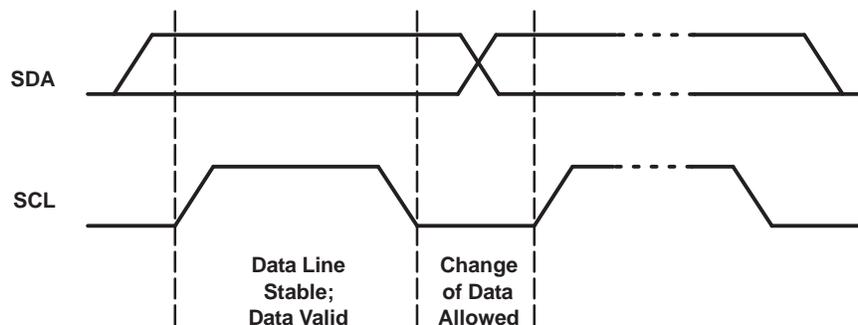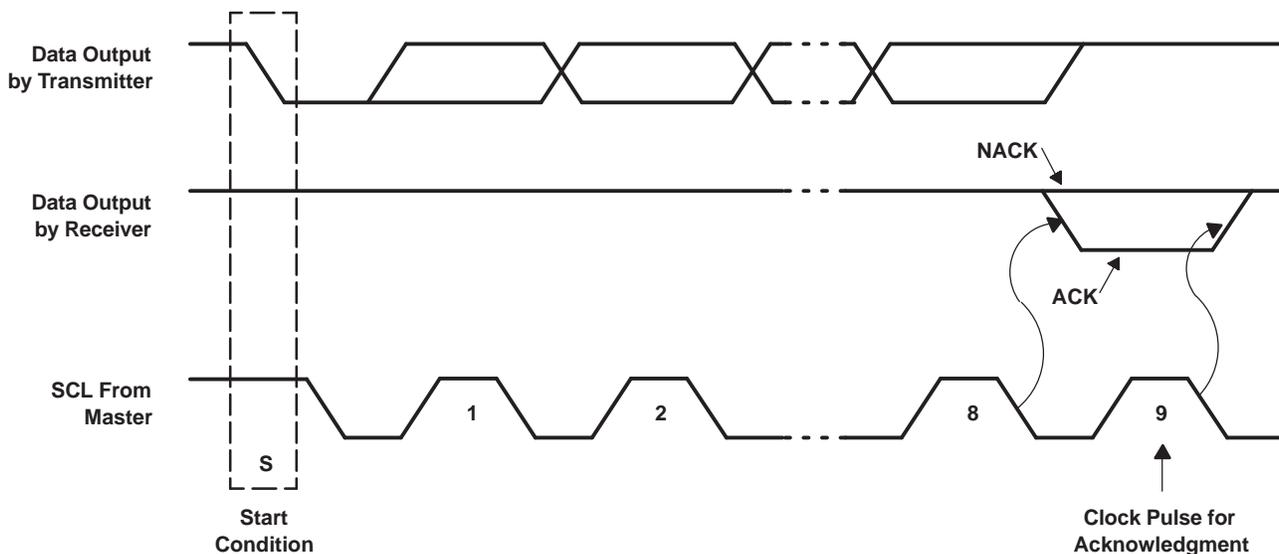
Figure 3. Acknowledgment on I^{2}C Bus

Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^{2}C slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

PCA9535

Device Address

Figure 4 shows the address byte of the PCA9535.
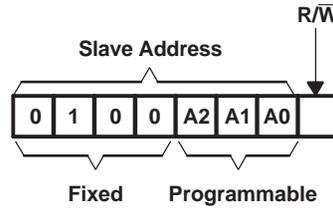
Figure 4. PCA9535 Address

Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9535. Three bits of this data byte state the operation (read or write) and the internal register (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.
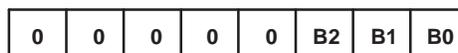
Figure 5. Control Register Bits

Control Register

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read/write byte	1111 1111
0	1	1	0x03	Output Port 1	Read/write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read/write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read/write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read/write byte	1111 1111

Register Descriptions

The Input Port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I²C device know that the Input Port registers will be accessed next.

Registers 0 and 1 (Input Port Registers)

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Registers 2 and 3 (Output Port Registers)

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding pin's original polarity is retained.

Registers 4 and 5 (Polarity Inversion Registers)

Bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0
Bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Registers 6 and 7 (Configuration Registers)

Bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1
Bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9535 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released, and the PCA9535 registers and I²C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Interrupt ($\overline{\text{INT}}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{\text{INT}}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt or in a Stop event. Resetting occurs in the read mode at the acknowledge (ACK) bit or not acknowledge (NACK) bit after the falling edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or vice versa.

$\overline{\text{INT}}$ has an open-drain structure and requires a pullup resistor to V_{CC}.

Bus Transactions

Data is exchanged between the master and the PCA9535 through write and read commands.

Writes

Data is transmitted to the PCA9535 by sending the device address and setting the least-significant bit to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the PCA9535 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversions, and Configurations. After sending data to one register, the next data byte is sent to the other register in the pair (see Figure 6 and Figure 7). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.
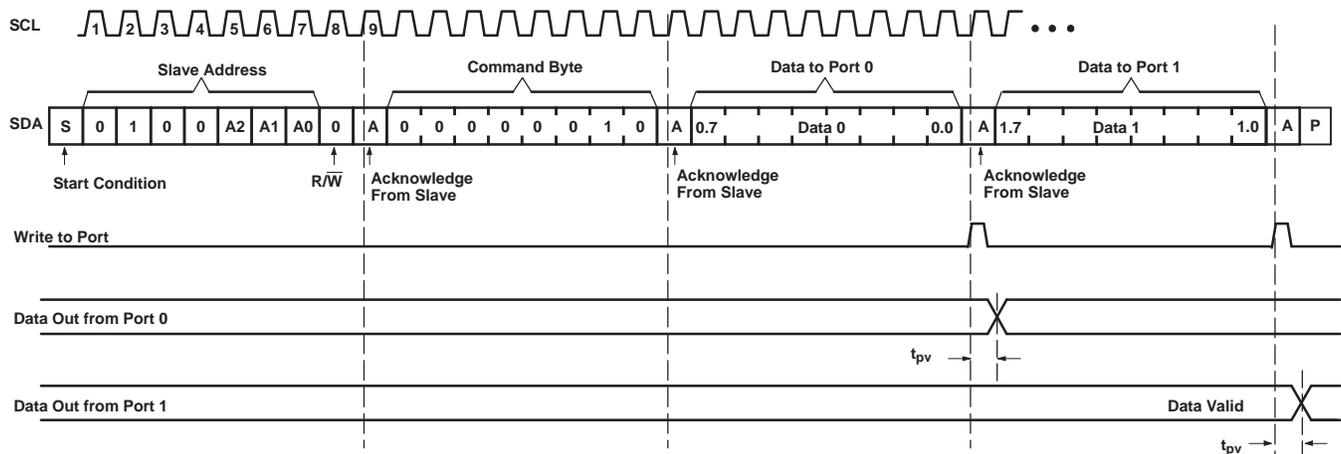

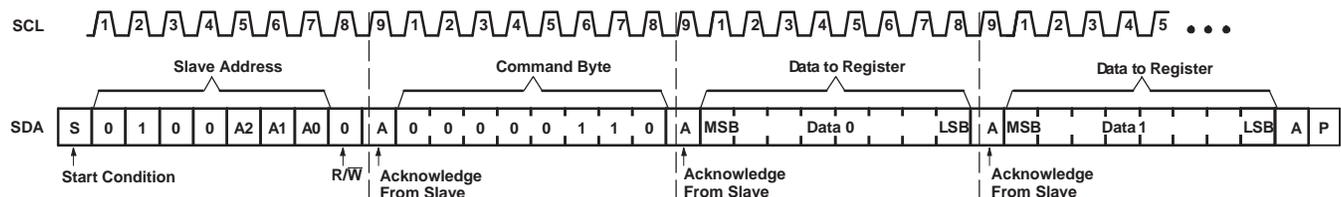**Figure 6. Write to Output Port Registers**

Figure 7. Write to Configuration Registers

Product Folder Link(s): *PCA9535*

Reads

The bus master first must send the PCA9535 address with the least-significant bit set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9535 (see Figure 8 through Figure 10).

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data
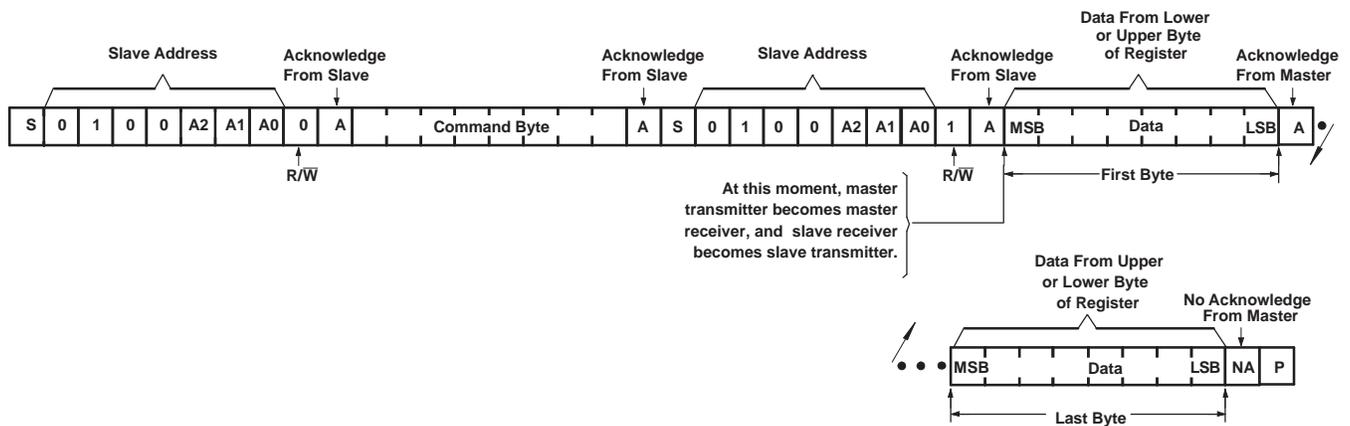
Figure 8. Read From Register
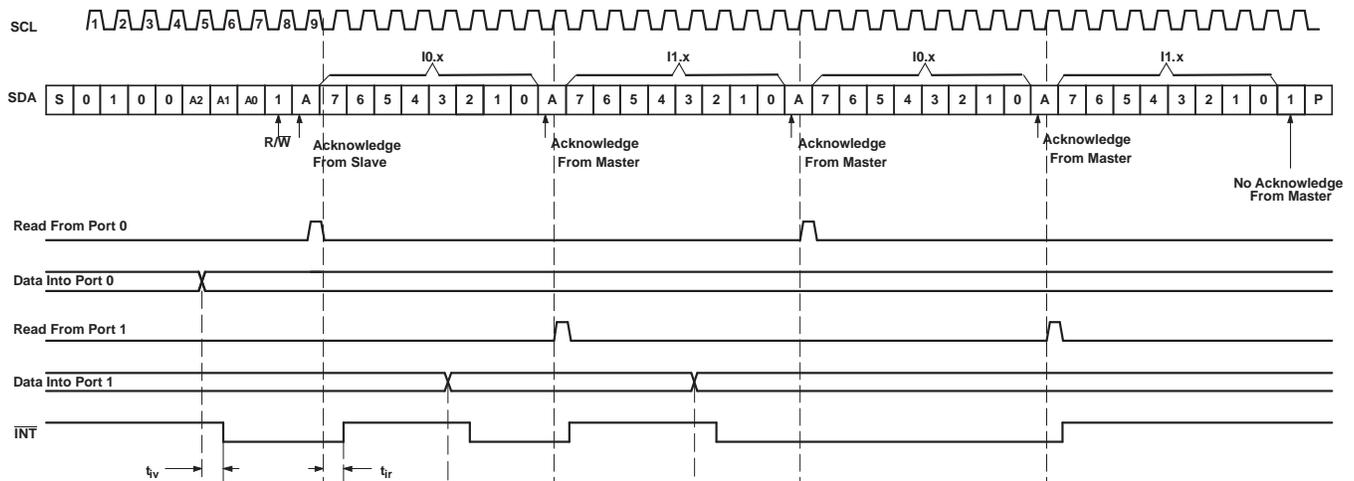
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Product Folder Link(s): *PCA9535*

A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 8 for these details).

Figure 9. Read Input Port Register, Scenario 1
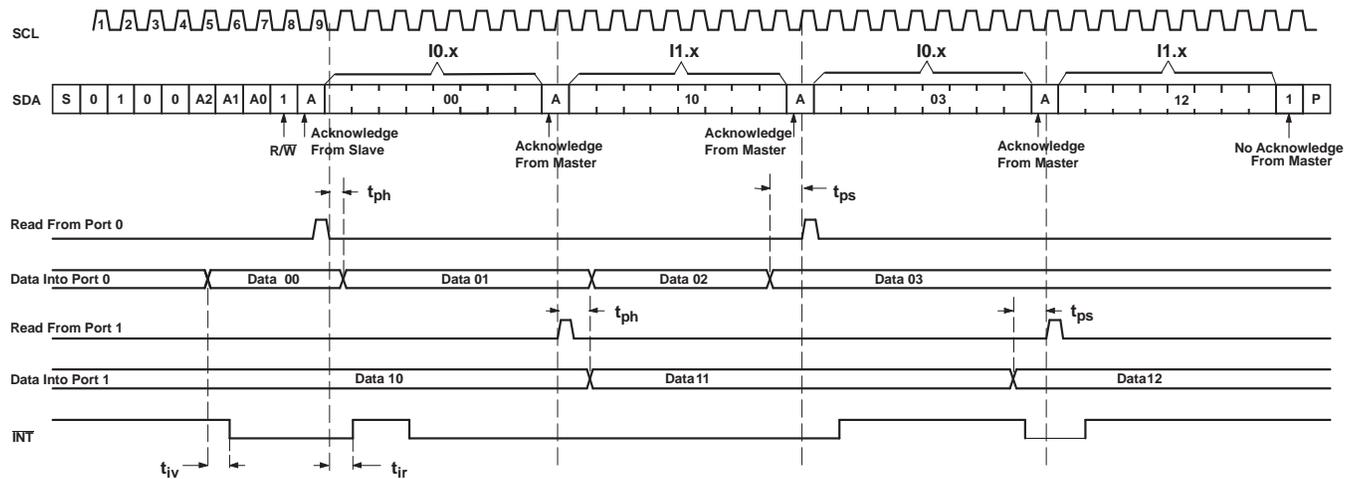
A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 8 for these details).

Figure 10. Read Input Port Register, Scenario 2

Product Folder Link(s): PCA9535

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6	V
V_I	Input voltage range[2]		−0.5	6	V
V_O	Output voltage range[2]		−0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		−50	mA
I_{CC}	Continuous current through GND			−250	mA
	Continuous current through V_{CC}			160	
θ_{JA}	Package thermal impedance, junction to free air[3]	DB package		63	°C/W
		DBQ package		61	
		DGV package		86	
		DW package		46	
		PW package		88	
		RGE package		45	
		RTW package		66	
θ_{JP}	Package thermal impedance, junction to pad	RGE package		1.5	°C/W
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		A2–A0, P07–P00, P17–P10	$0.7 \times V_{CC}$	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	−0.5	$0.3 \times V_{CC}$	V
		A2–A0, P07–P00, P17–P10	−0.5	$0.3 \times V_{CC}$	
I_{OH}	High-level output current	P07–P00, P17–P10		−10	mA
I_{OL}	Low-level output current	P07–P00, P17–P10		25	mA
T_A	Operating free-air temperature		−40	85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18$ mA	2.3 V to 5.5 V	−1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, $I_O = 0$	V_{POR}		1.5	1.65	V
V_{OH}	P-port high-level output voltage[2]	$I_{OH} = -8$ mA	2.3 V	1.8			V
			3 V	2.6			
			4.75 V	4.1			
		$I_{OH} = -10$ mA	2.3 V	1.7			
			3 V	2.5			
			4.75 V	4			
I_{OL}	SDA	$V_{OL} = 0.4$ V	2.3 V to 5.5 V	3			mA
	P port[3]	$V_{OL} = 0.5$ V		8	20		
		$V_{OL} = 0.7$ V		10	24		
	$\overline{INT}$	$V_{OL} = 0.4$ V		3			
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	µA
	A2–A0					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	µA
I_{IL}	P port	$V_I = $ GND	2.3 V to 5.5 V			−1	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, $f_{SCL} = 400$ kHz	5.5 V		100	200	µA
			3.6 V		30	75	
			2.7 V		20	50	
	Standby mode	$V_I = $ GND, $I_O = 0$, I/O = inputs, $f_{SCL} = 0$ kHz	5.5 V		0.5	1	
			3.6 V		0.4	0.9	
			2.7 V		0.25	0.8	
ΔI_{CC}	Additional current in standby mode	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			200	µA
C_I	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		3	7	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		3	7	pF
	P port				3.7	9.5	

(1)　All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and $T_A = 25°C$.
(2)　Each I/O must be limited externally to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
(3)　The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

I²C INTERFACE TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 11)

			MIN	MAX	UNIT
t_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		$20 + 0.1C_b$ [(1)]	300	ns
t_{icf}	I²C input fall time		$20 + 0.1C_b$ [(1)]	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	$20 + 0.1C_b$ [(1)]	300	ns
t_{buf}	I²C bus free time between Stop and Start		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		0.6		µs
t_{sps}	I²C Stop condition setup		0.6		µs
$t_{vd(data)}$	Valid-data time	SCL low to SDA output valid	50		ns
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.1	0.9	µs
C_b	I²C bus capacitive load			400	pF

(1) C_b = total capacitance of one bus line in pF

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L \le 100$ pF (unless otherwise noted) (see Figure 12 and Figure 13)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs
t_{pv}	Output data valid	SCL	P port		200	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

TYPICAL CHARACTERISTICS

$T_A = 25°C$ (unless otherwise noted)

SUPPLY CURRENT vs TEMPERATURE

STANDBY SUPPLY CURRENT vs TEMPERATURE

SUPPLY CURRENT vs SUPPLY VOLTAGE
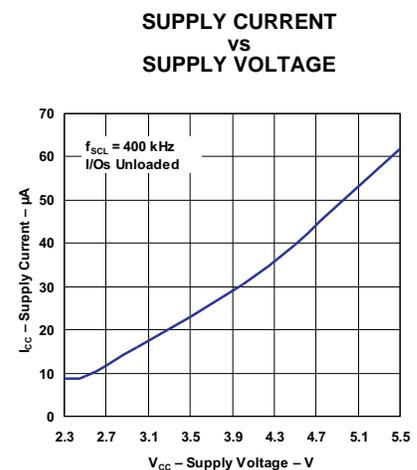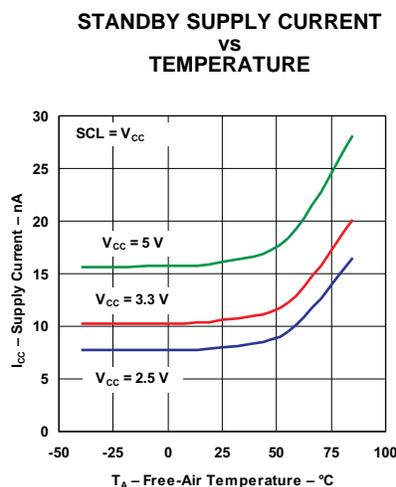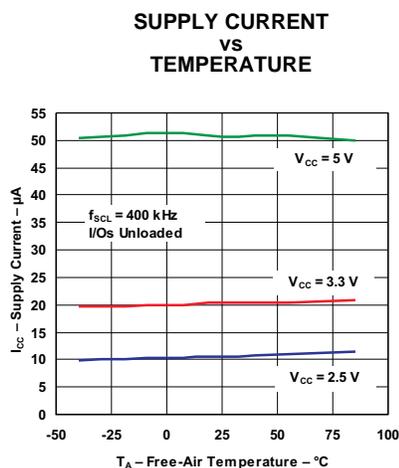
TYPICAL CHARACTERISTICS (continued)

$T_A = 25°C$ (unless otherwise noted)

I/O SINK CURRENT
vs
OUTPUT LOW VOLTAGE

I/O SINK CURRENT
vs
OUTPUT LOW VOLTAGE

I/O SINK CURRENT
vs
OUTPUT LOW VOLTAGE

I/O OUTPUT LOW VOLTAGE
vs
TEMPERATURE

I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE

I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE

I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE

I/O HIGH VOLTAGE
vs
TEMPERATURE

OUTPUT HIGH VOLTAGE
vs
SUPPLY VOLTAGE
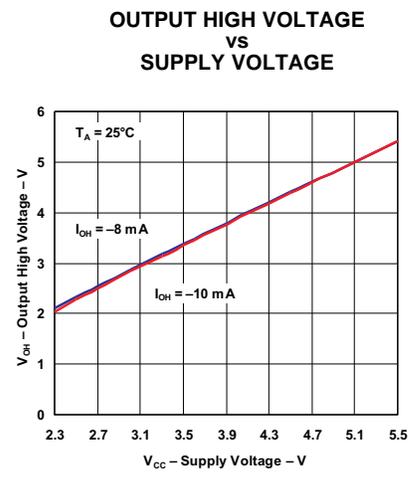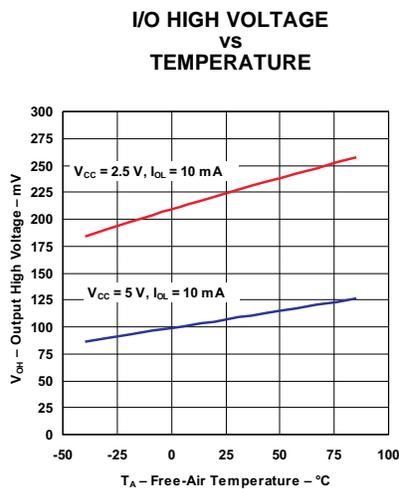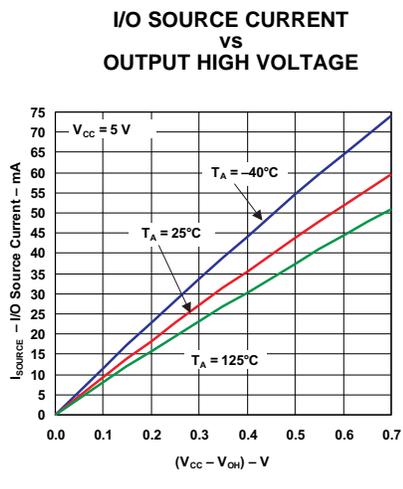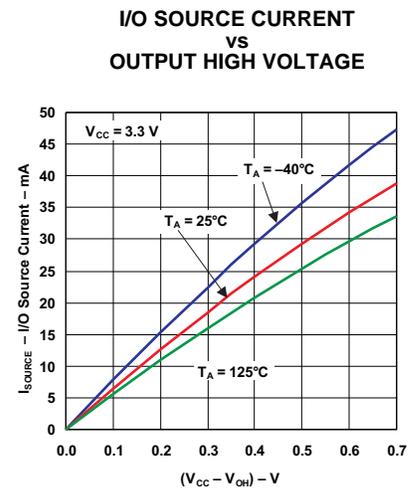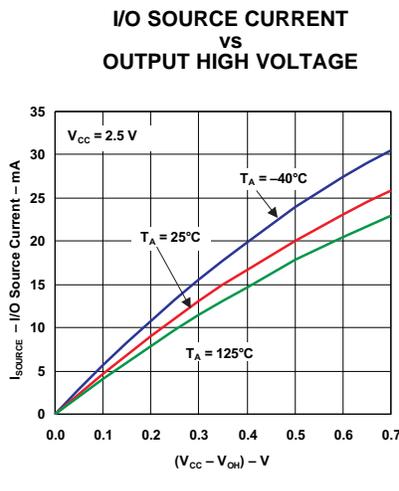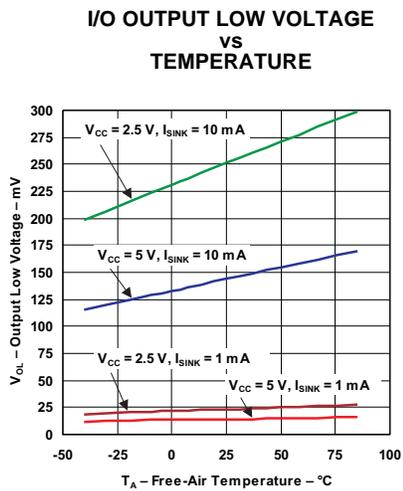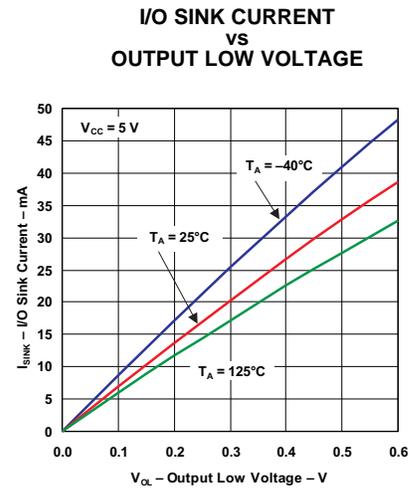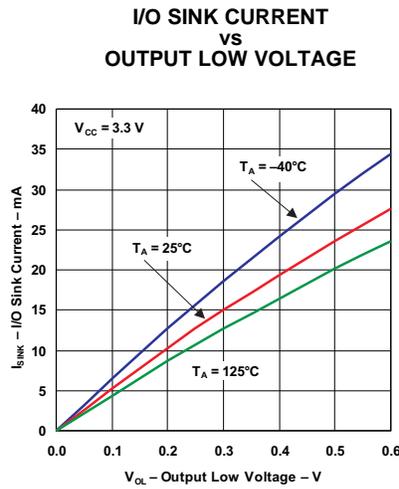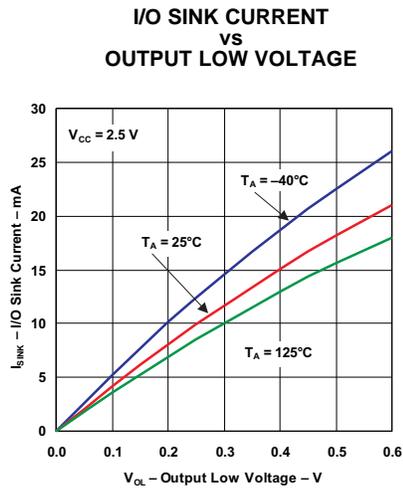
PARAMETER MEASUREMENT INFORMATION
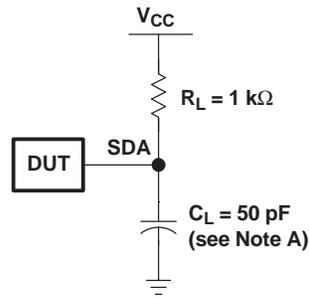
SDA LOAD CONFIGURATION
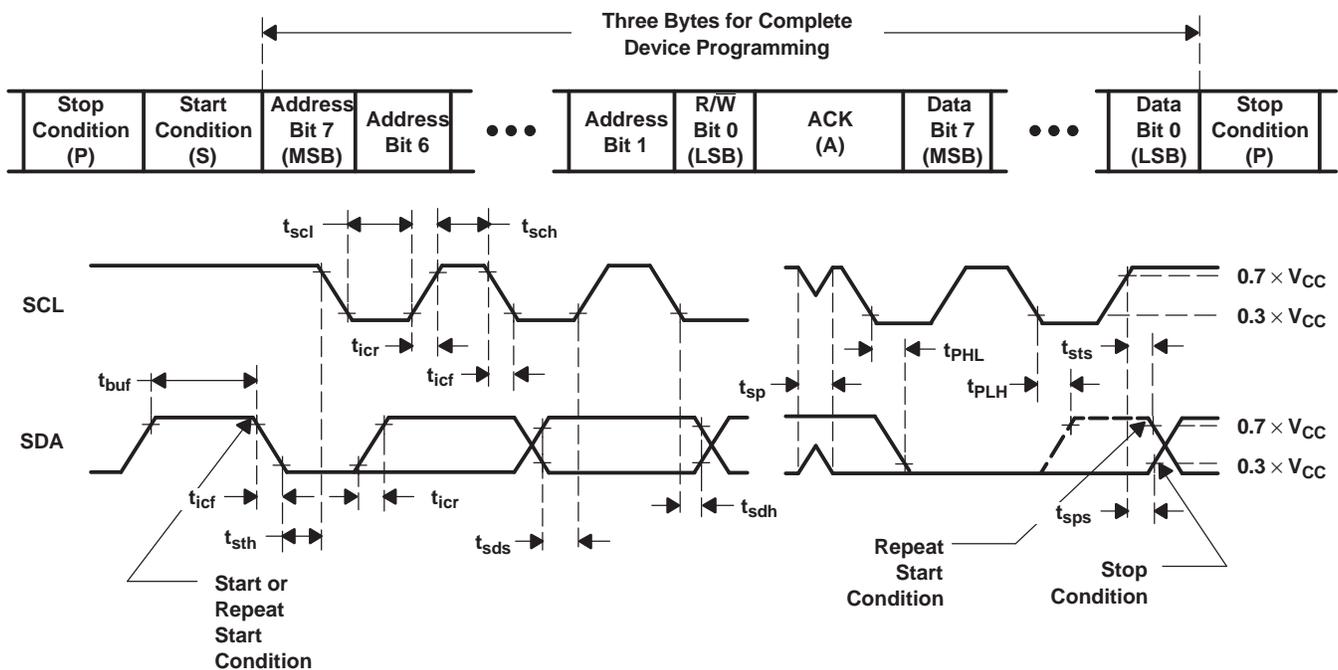
VOLTAGE WAVEFORMS

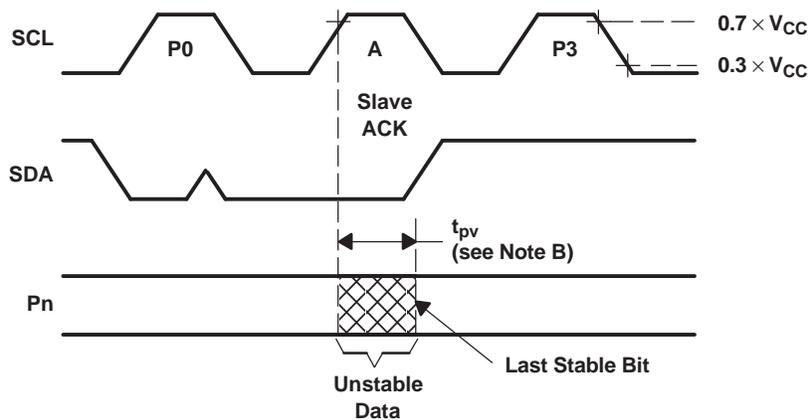| BYTE	DESCRIPTION
1	I^{2}C address
2, 3	P-port data

A.   C$_L$ includes probe and jig capacitance.

B.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z$_O$ = 50 Ω, t$_r$/t$_f$ ≤ 30 ns.

C.   All parameters and waveforms are not applicable to all devices.

Figure 11. I^{2}C Interface Load Circuit and Voltage Waveforms
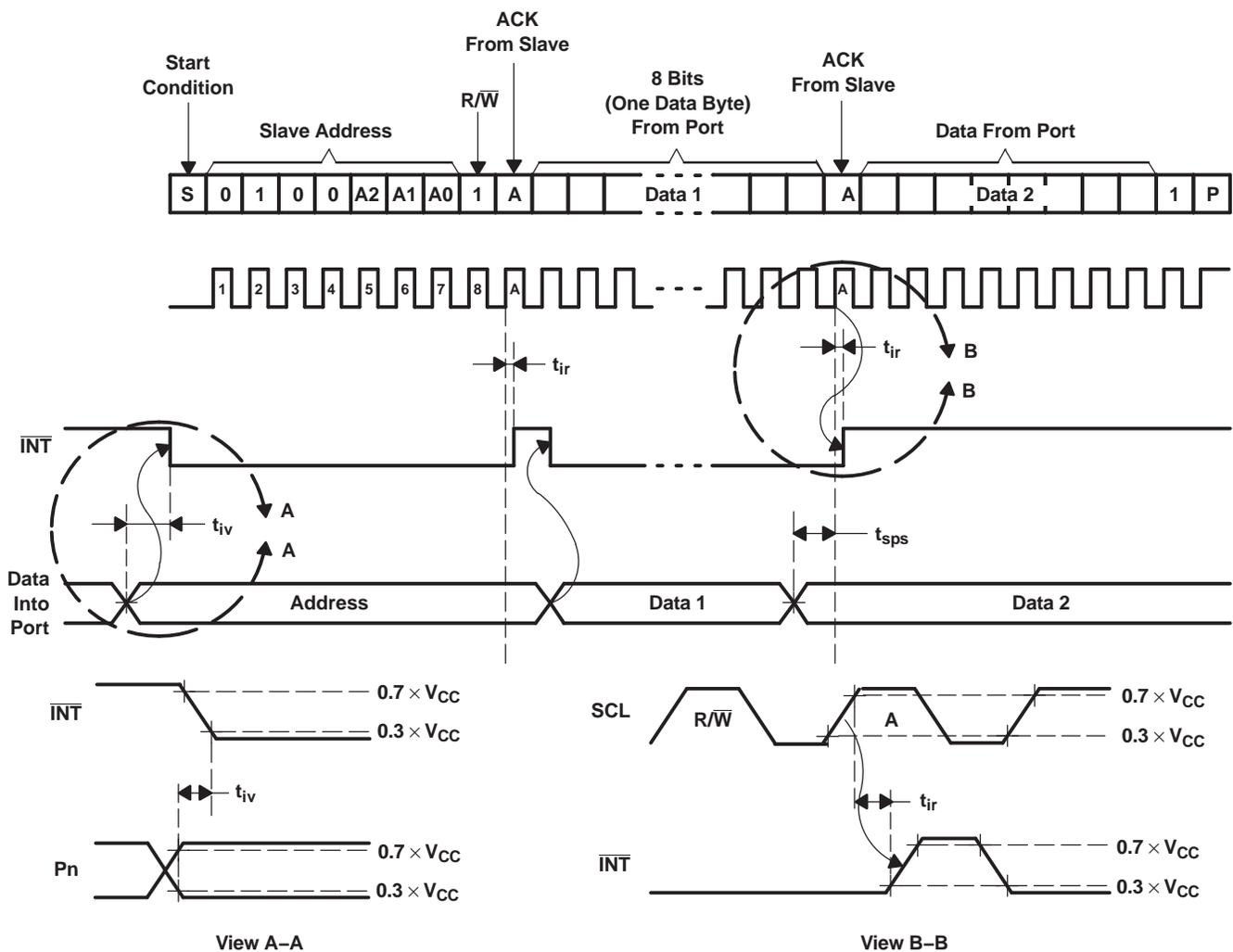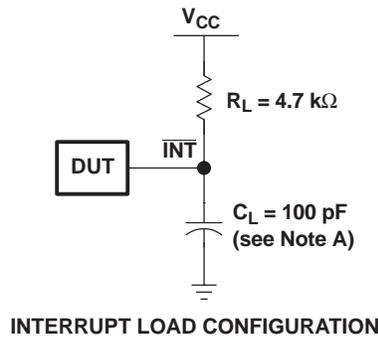
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PARAMETER MEASUREMENT INFORMATION (continued)

INTERRUPT LOAD CONFIGURATION

View A−A

View B−B

A. C_L includes probe and jig capacitance.

B.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C.   All parameters and waveforms are not applicable to all devices.
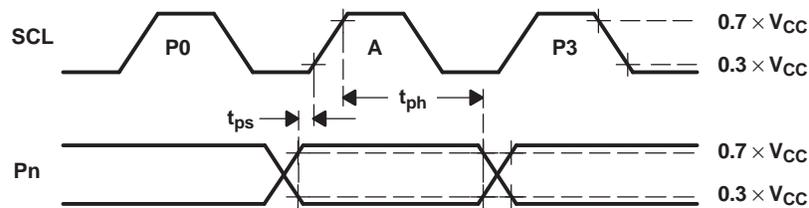
Figure 12. Interrupt Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)
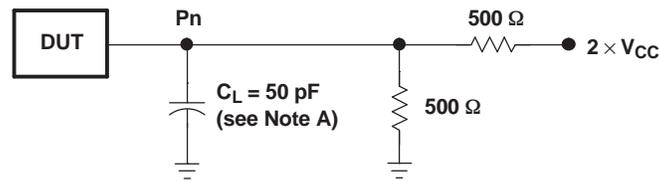
P-PORT LOAD CONFIGURATION


WRITE MODE (R/$\overline{W}$ = 0)

READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O (Pn) output.

C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 13. P-Port Load Circuit and Voltage Waveforms
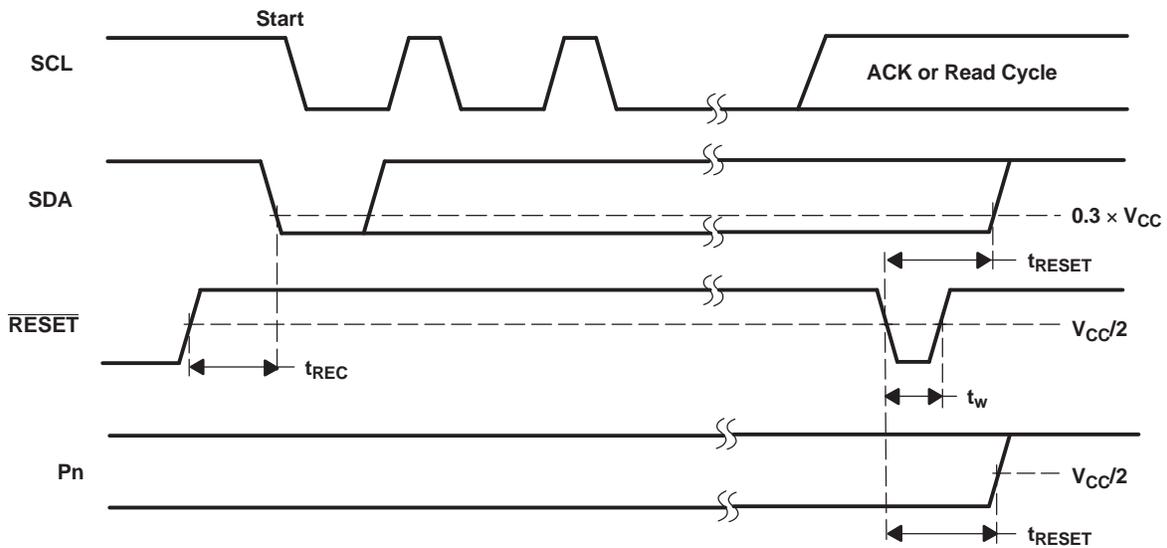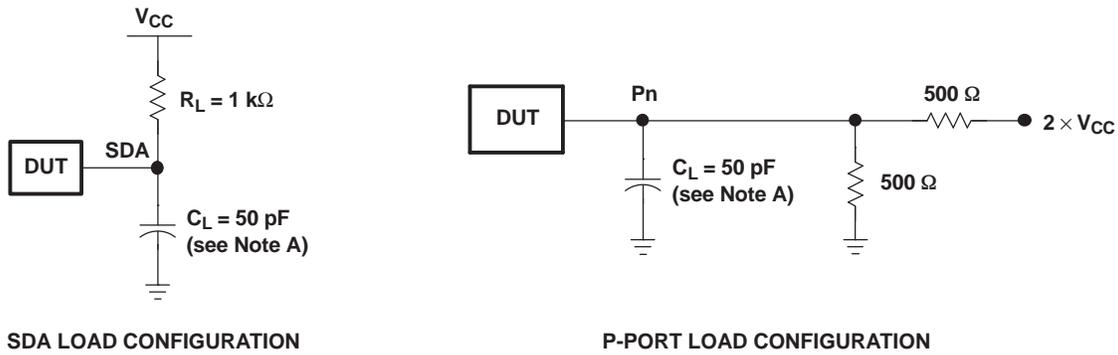
PARAMETER MEASUREMENT INFORMATION (continued)

SDA LOAD CONFIGURATION

P-PORT LOAD CONFIGURATION


A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

D. I/Os are configured as inputs.

E. All parameters and waveforms are not applicable to all devices.

Figure 14. Reset Load Circuits and Voltage Waveforms

Product Folder Link(s): *PCA9535*

APPLICATION INFORMATION

Figure 15 shows an application in which the PCA9535 can be used.
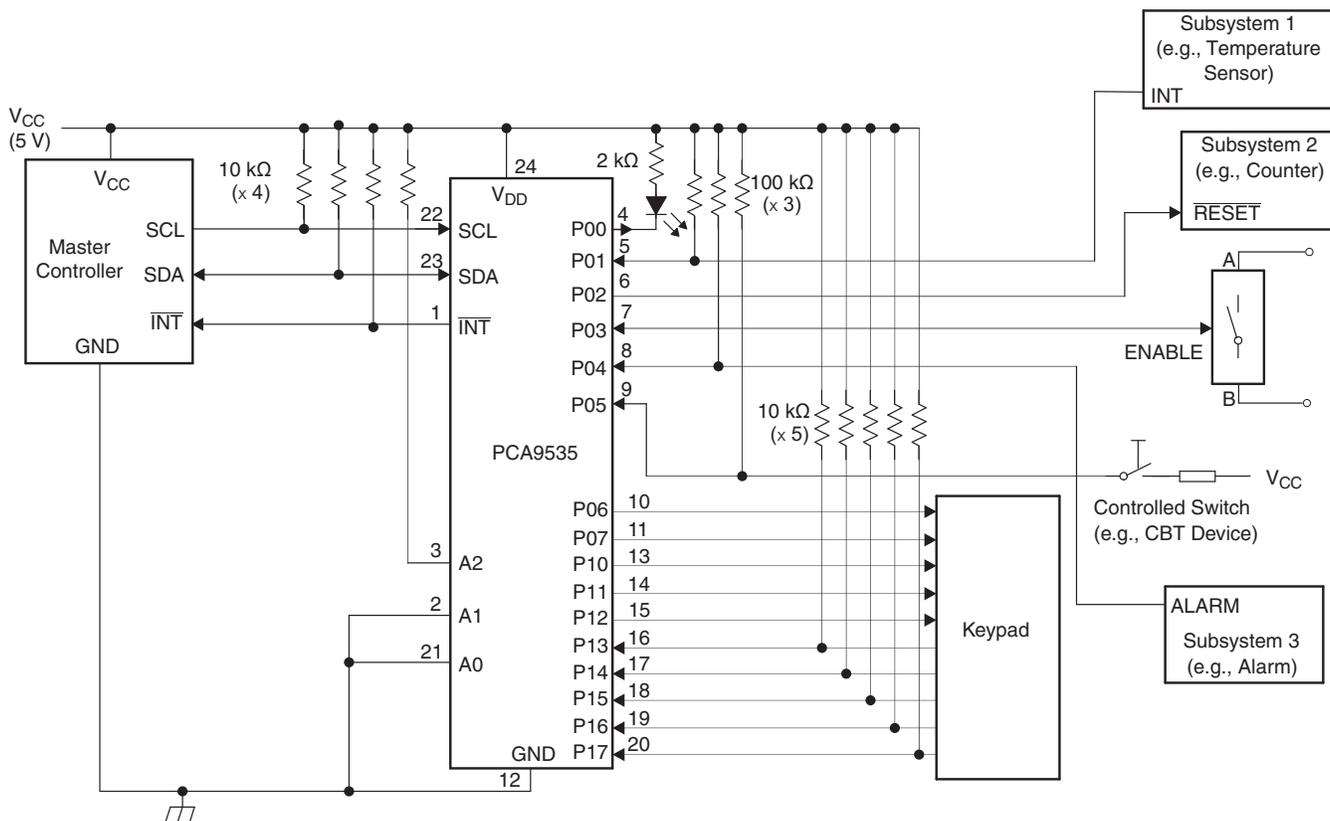
A. Device address is configured as 0100100 for this example.
B. P00, P02, and P03 are configured as outputs.
C. P01, P04–P07, and P10–P17 are configured as inputs.
D. Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.

Figure 15. Typical Application

Minimizing I_{CC} When I/O Is Used to Control LED

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor as shown in Figure 15. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in Electrical Characteristics shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC}, when the LED is off, to minimize current consumption.

Figure 16 shows a high-value resistor in parallel with the LED. Figure 17 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.
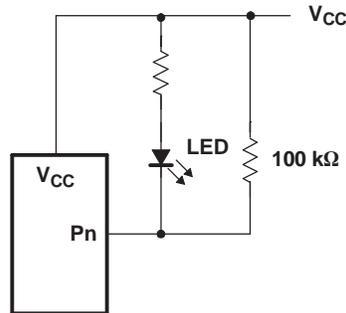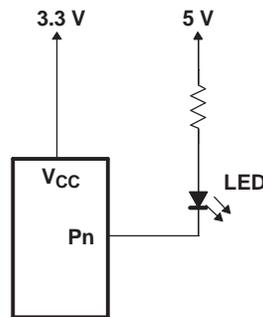

Figure 16. High-Value Resistor in Parallel With LED

Figure 17. Device Supplied by Lower Voltage

Product Folder Link(s): *PCA9535*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
PCA9535DB	NRND	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535DBG4	NRND	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535DBQR	NRND	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Samples Not Available
PCA9535DBQRG4	NRND	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Samples Not Available
PCA9535DBR	NRND	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535DBRG4	NRND	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535DGVR	NRND	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535DGVRG4	NRND	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535DW	NRND	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535DWG4	NRND	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535DWR	NRND	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535DWRG4	NRND	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535PW	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535PWE4	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535PWG4	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535PWR	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535PWRE4	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
PCA9535PWRG4	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Samples Not Available
PCA9535RGER	NRND	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Samples Not Available
PCA9535RGERG4	NRND	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Samples Not Available
PCA9535RTWR	NRND	QFN	RTW	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Samples Not Available
PCA9535RTWRG4	NRND	QFN	RTW	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Samples Not Available

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
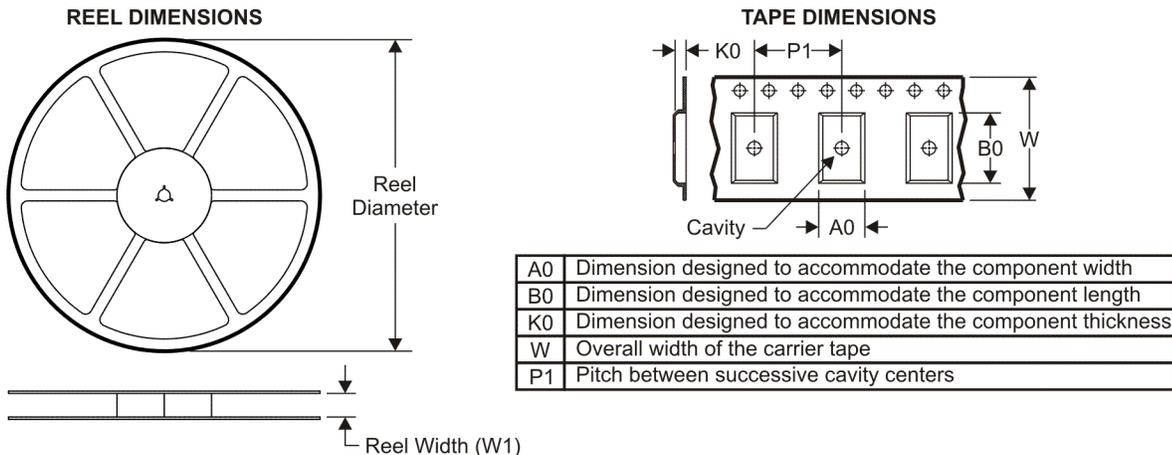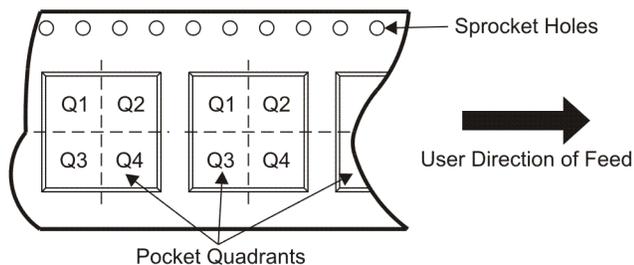**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9535DBQR	SSOP/QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCA9535DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCA9535DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9535DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCA9535PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCA9535RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCA9535RTWR	QFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS
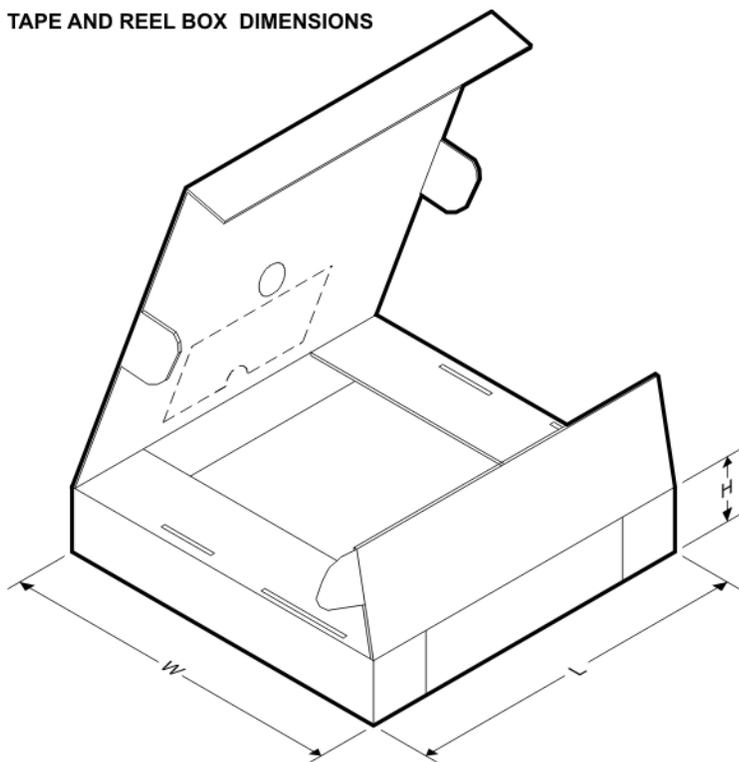
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9535DBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
PCA9535DBR	SSOP	DB	24	2000	346.0	346.0	33.0
PCA9535DGVR	TVSOP	DGV	24	2000	346.0	346.0	29.0
PCA9535DWR	SOIC	DW	24	2000	346.0	346.0	41.0
PCA9535PWR	TSSOP	PW	24	2000	346.0	346.0	33.0
PCA9535RGER	VQFN	RGE	24	3000	346.0	346.0	29.0
PCA9535RTWR	QFN	RTW	24	3000	346.0	346.0	29.0

DW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°–8°

0.050 (1,27)
0.016 (0,40)

4040000−5/G 01/11
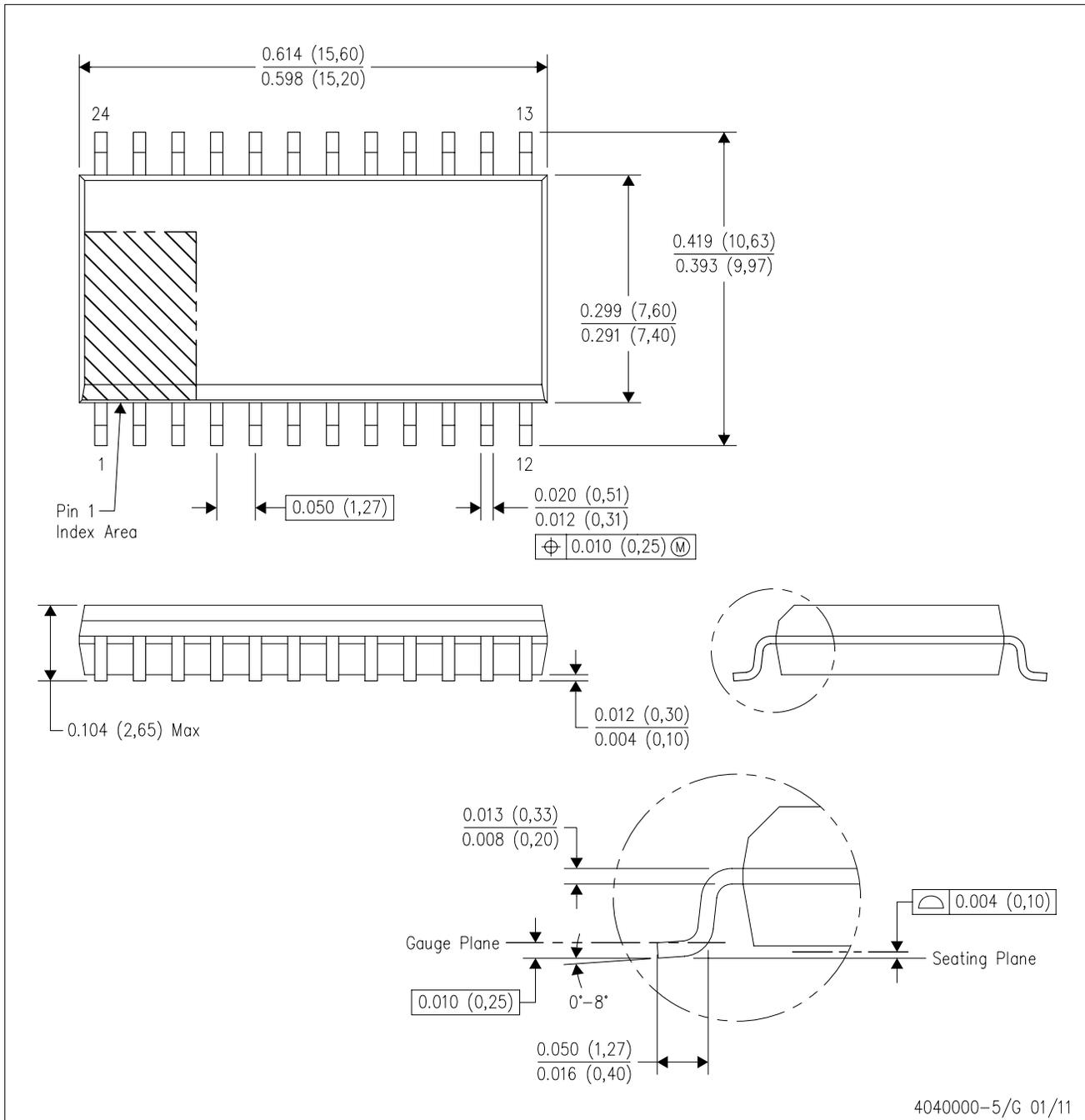
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AD.

DBQ (R−PDSO−G24)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

24   13

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   12

Pin 1
Index Area

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−4/H   10/2008
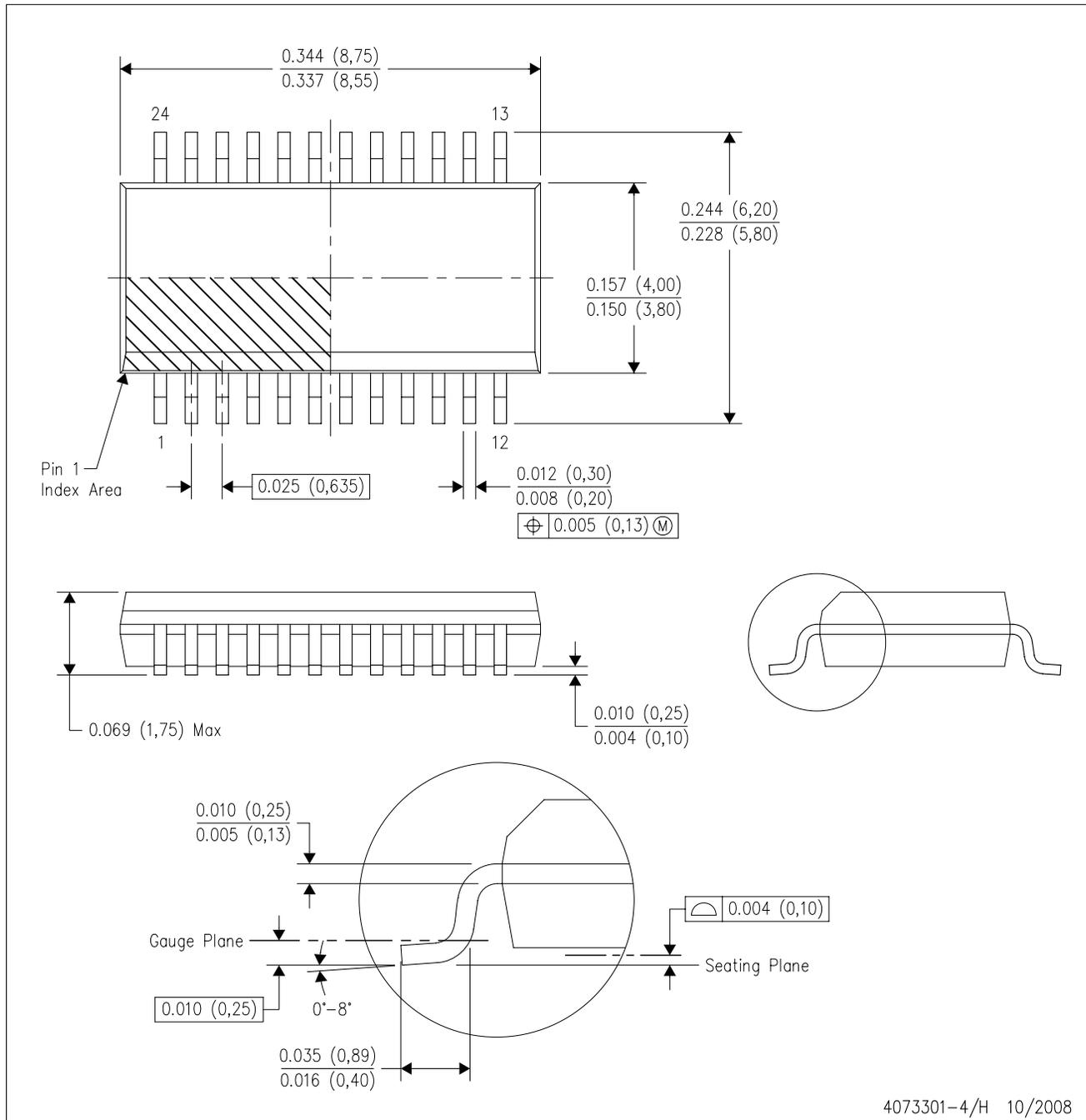
NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
         D. Falls within JEDEC MO−137 variation AE.

DBQ (R−PDSO−G24)   PLASTIC SMALL OUTLINE PACKAGE
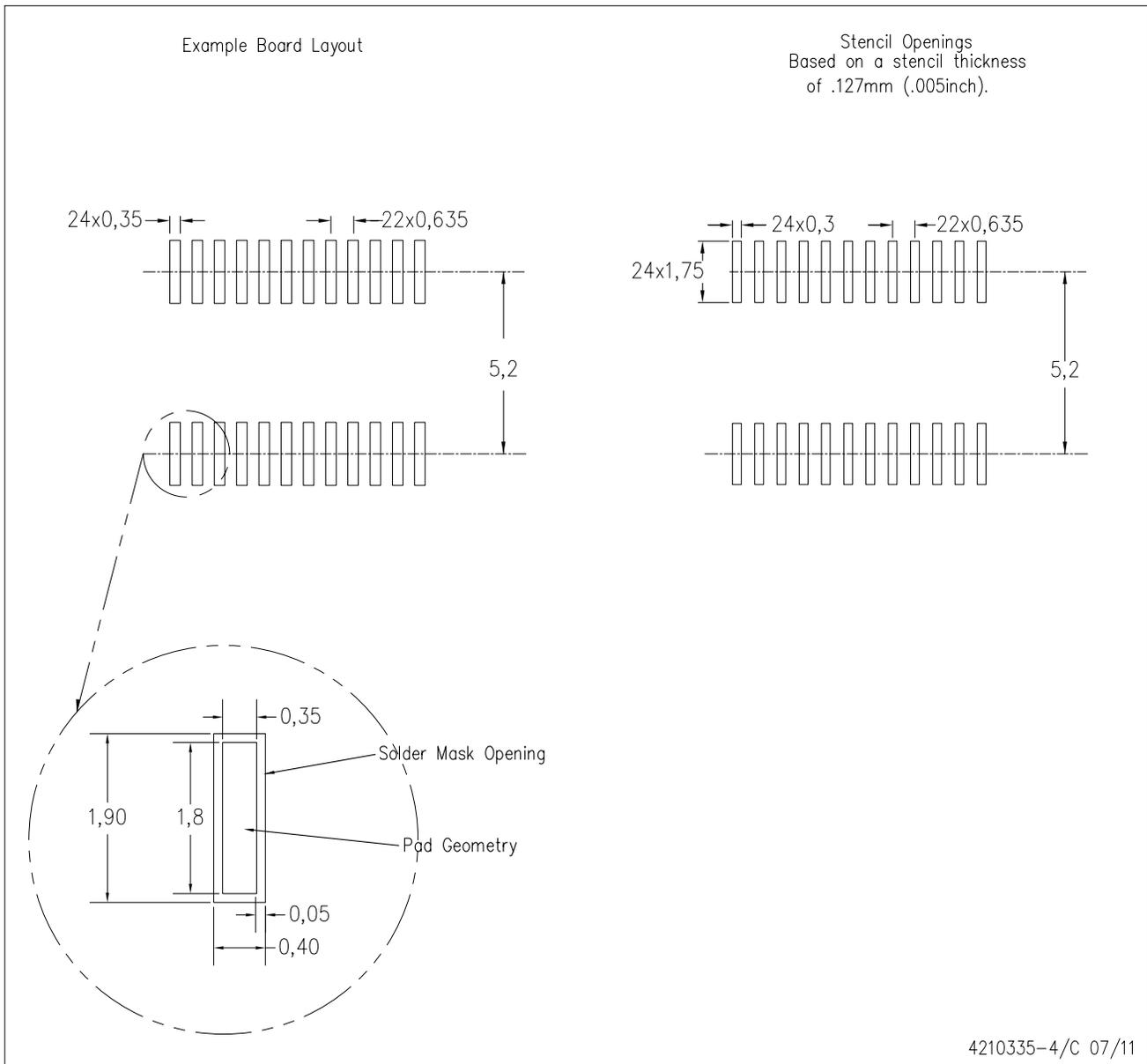
Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

24x0,35 — | |←   → | |←22x0,635

5,2

24x0,3 — | |←   → | |←22x0,635

24x1,75

5,2

0,35

Solder Mask Opening

1,90   1,8

Pad Geometry

0,05

0,40

4210335−4/C 07/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC−7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

PW (R−PDSO−G24)   PLASTIC SMALL OUTLINE
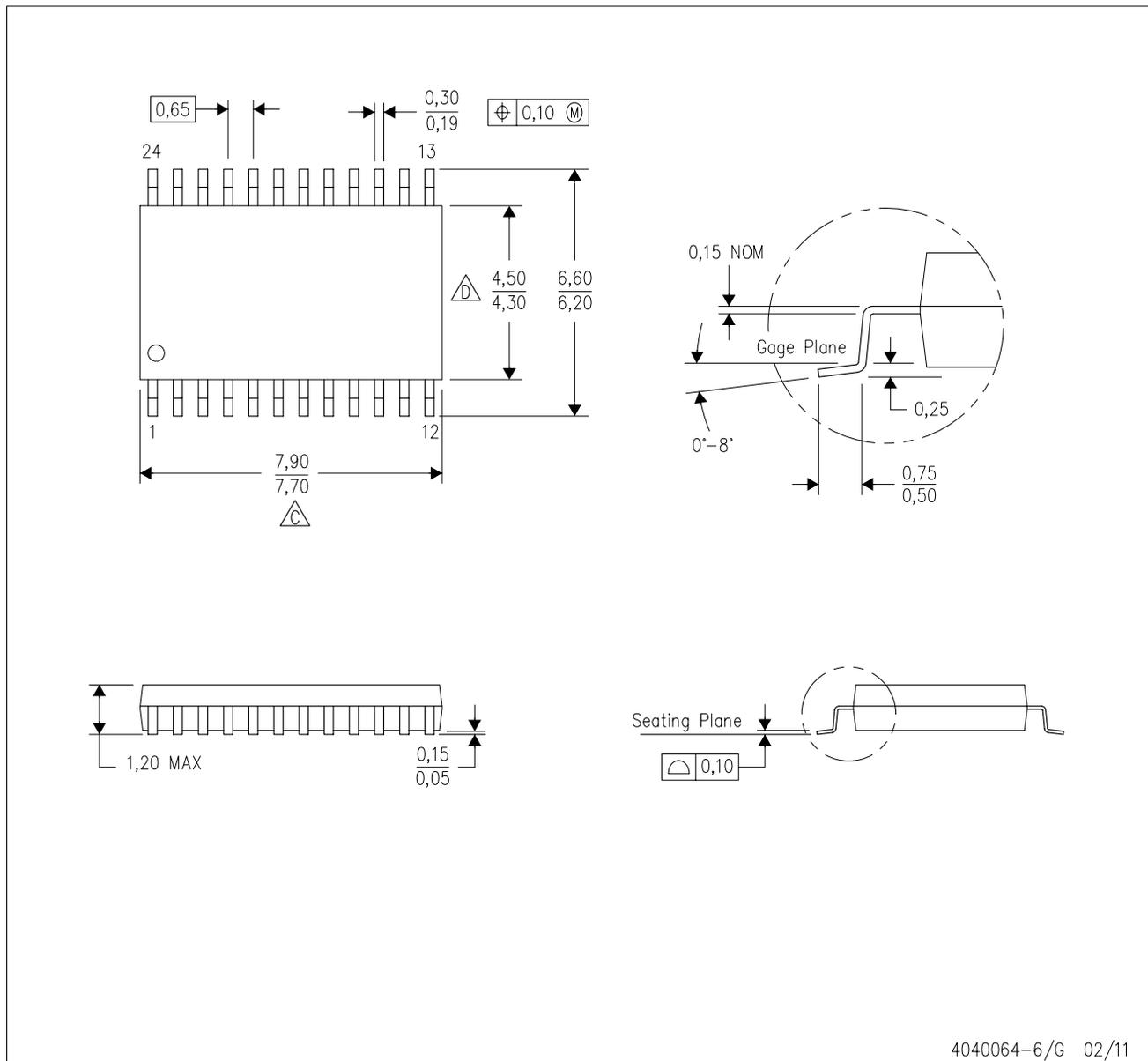
4040064−6/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153
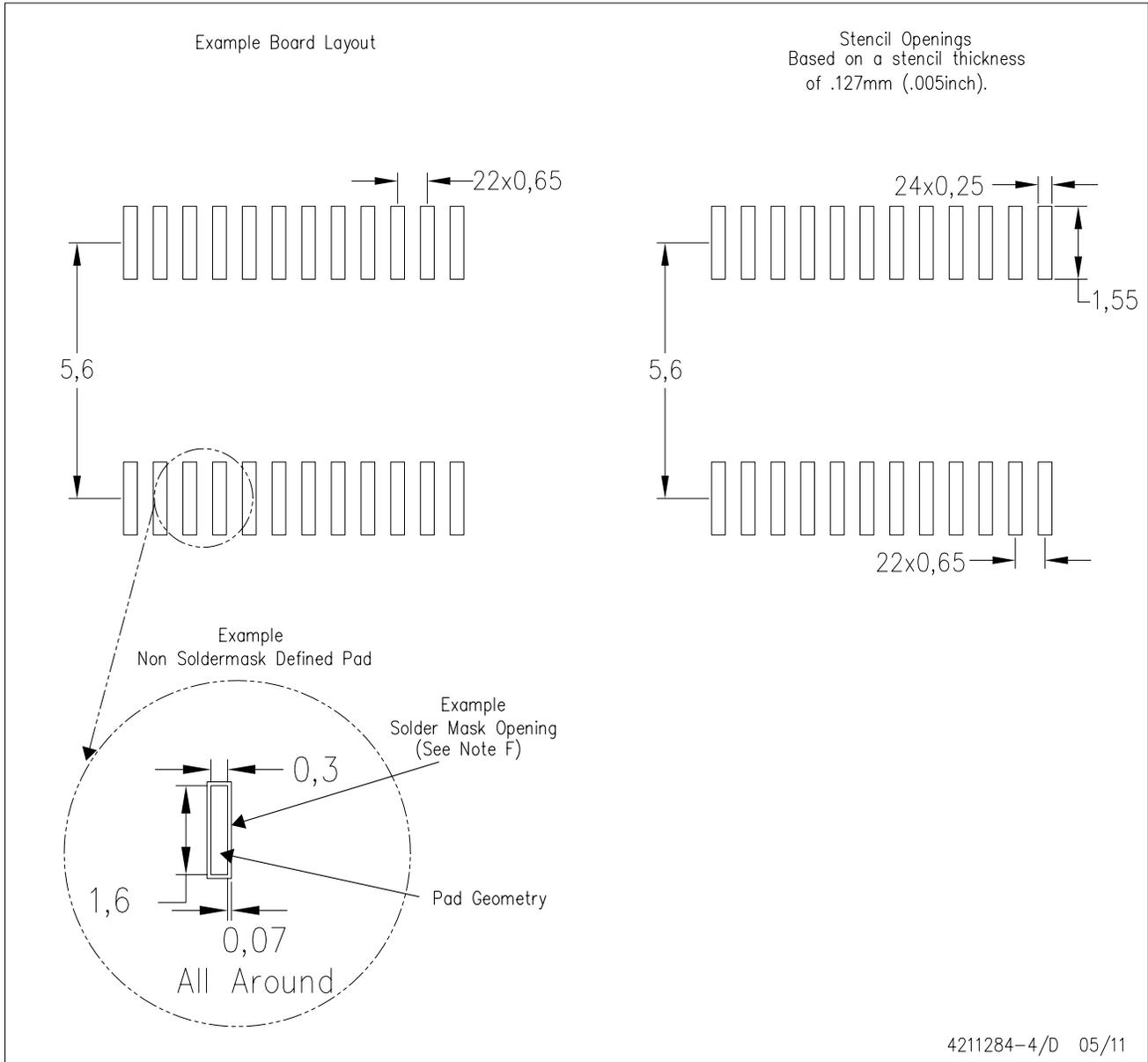
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PW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

22x0,65

5,6

24x0,25

5,6

1,55

22x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
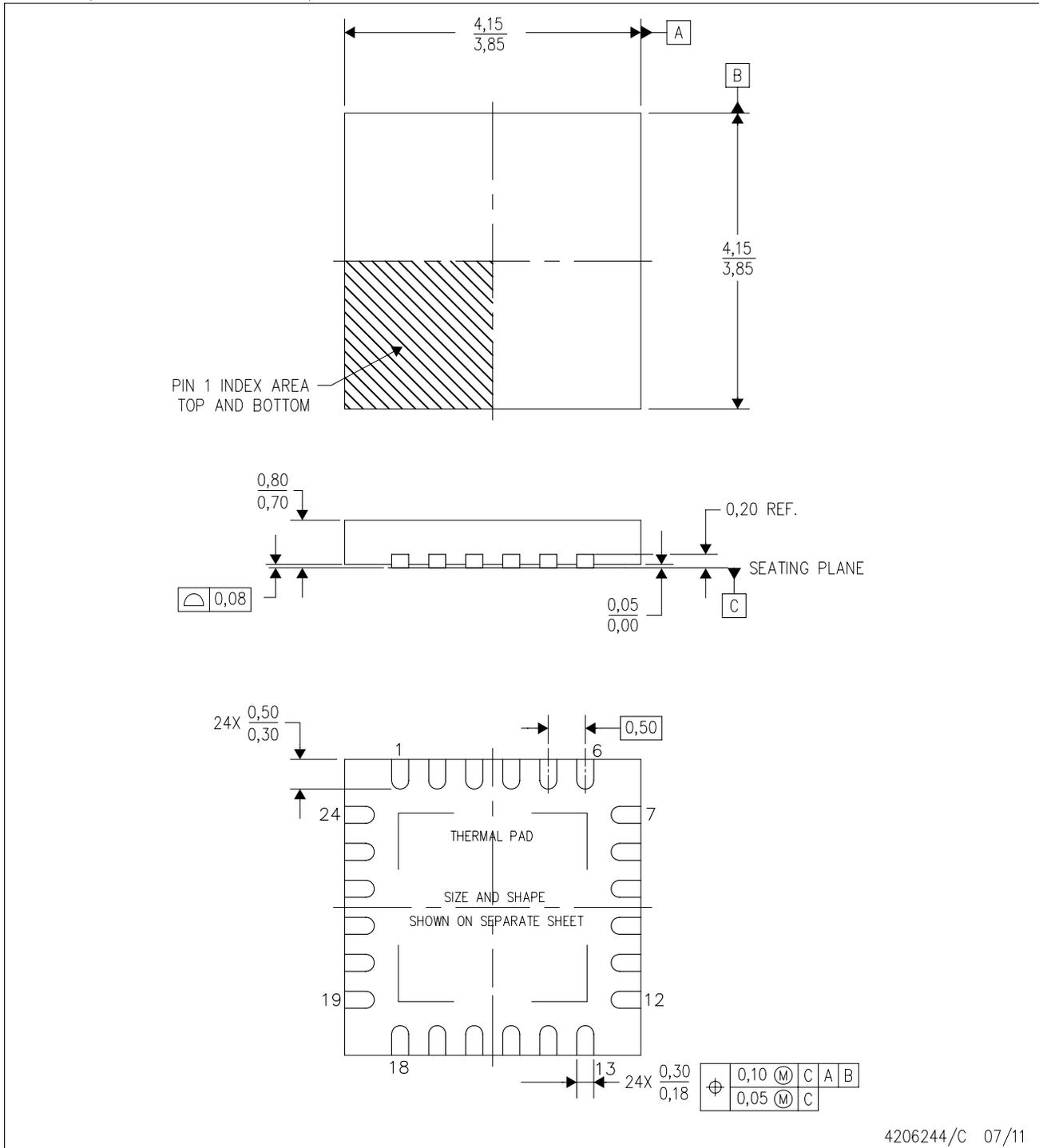(See Note F)

0,3

1,6

0,07

All Around

Pad Geometry

4211284−4/D   05/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGE (S−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{4,15}{3,85}$

$\frac{4,15}{3,85}$

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

$\frac{0,05}{0,00}$

△ 0,08

0,50

24X $\frac{0,50}{0,30}$

1   6

24   7

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

19   12

18   13

24X $\frac{0,30}{0,18}$

⊕	0,10 Ⓜ	C	A	B
	0,05 Ⓜ	C		

4204104/G 07/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Quad Flatpack, No−Leads (QFN) package configuration.
        D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
        E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
        F. Falls within JEDEC MO−220.

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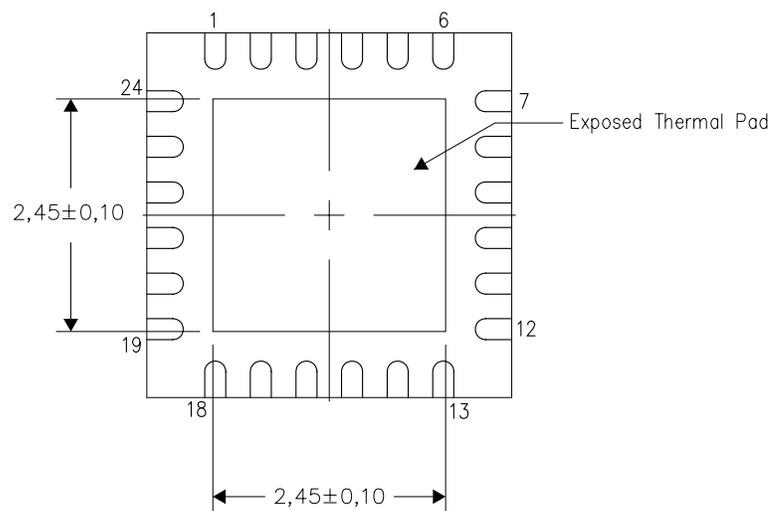RGE (S−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

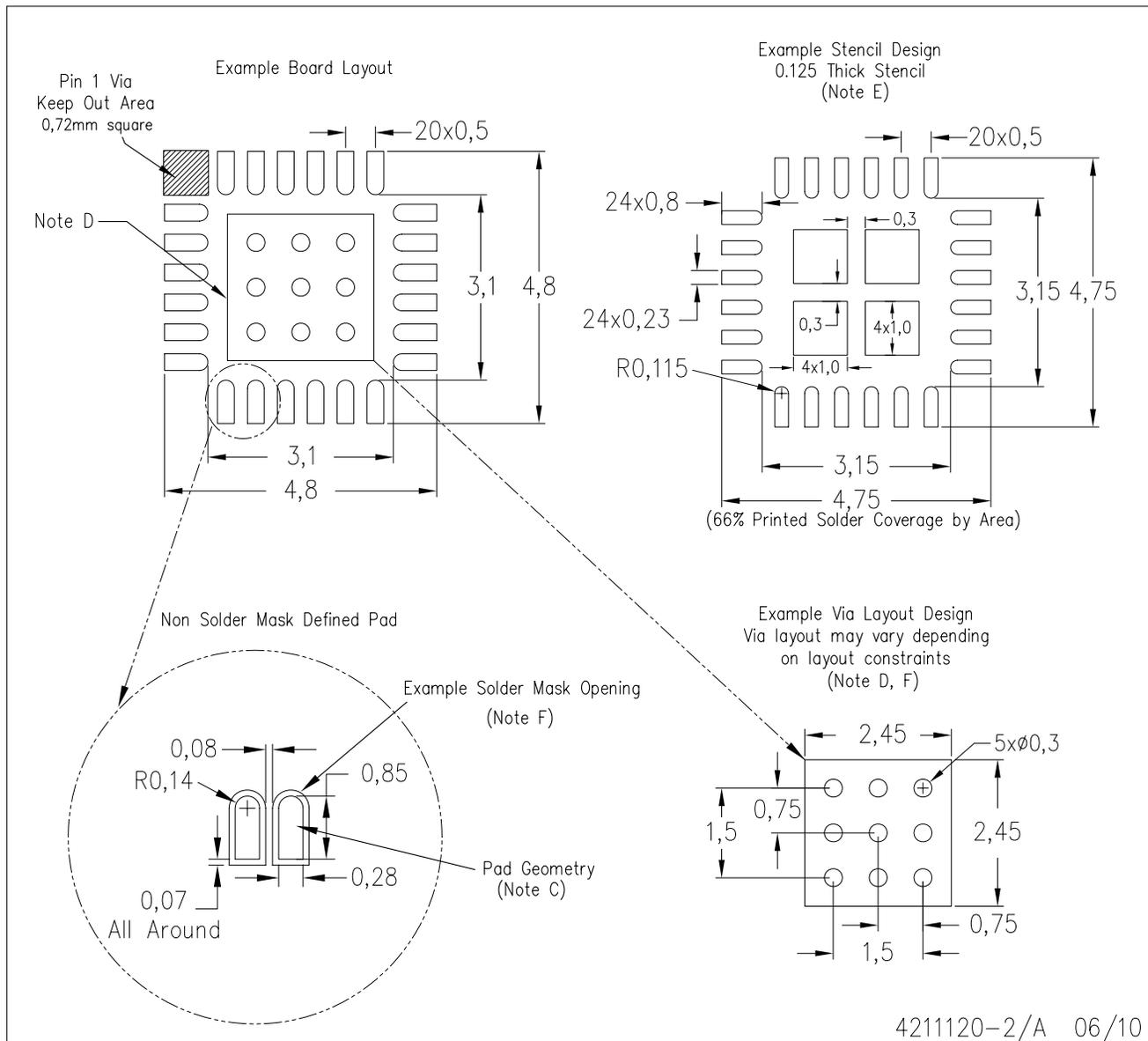The exposed thermal pad dimensions for this package are shown in the following illustration.

Bottom View

Exposed Thermal Pad Dimensions

4206344−6/Y 07/11

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24)   PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout

Pin 1 Via
Keep Out Area
0,72mm square

Note D

20x0,5

3,1   4,8

3,1

4,8

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07

0,28

Pad Geometry
(Note C)

All Around

Example Stencil Design
0.125 Thick Stencil
(Note E)

20x0,5

24x0,8

0,3

24x0,23

0,3

R0,115

4x0,825   4X0,825

3,15   4,75

3,15

4,75

(60% Printed Solder Coverage by Area)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

2,1   9xØ0,3

0,75

1,5   2,1

0,75

1,5

4207991–5/M   07/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board.   Refer to Application Note, Quad Flat–Pack
              Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout.   These documents are available at
              www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations.   Refer to IPC 7525 for stencil design
              considerations.
         F.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
              recommendations for vias placed in the thermal pad.

RTW (S−PWQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

4,15 / 3,85   A

B

4,15 / 3,85

PIN 1 INDEX AREA
TOP AND BOTTOM

0,80 / 0,70

0,20 REF.

SEATING PLANE

0,08

0,05 / 0,00   C

24X 0,50 / 0,30

0,50

1   6

24   7

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

19   12

18   13 24X 0,30 / 0,18

0,10 Ⓜ C A B
0,05 Ⓜ C

4206244/C 07/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−Leads (QFN) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   Falls within JEDEC MO−220.

RTW (S−PWQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Bottom View

Exposed Thermal Pad Dimensions

4206249−3/L 07/11

NOTES: A. All linear dimensions are in millimeters

RTW (S−PWQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Pin 1 Via
Keep Out Area
0,72mm square

Note D

20x0,5

3,1   4,8

3,1

4,8

Example Stencil Design
0.125 Thick Stencil
(Note E)

20x0,5

24x0,8

0,3

24x0,23

0,3   4x1,0

R0,115   4x1,0

3,15 4,75

3,15

4,75

(66% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07
All Around

0,28

Pad Geometry
(Note C)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

2,45

5x⌀0,3

0,75

1,5

2,45

0,75

1,5

4211120−2/A   06/10

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
             Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
             for specific thermal information, via requirements, and recommended board layout. These documents are available at
             www.ti.com <http://www.ti.com>.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design
             considerations.
         F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
             recommendations for vias placed in the thermal pad.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN
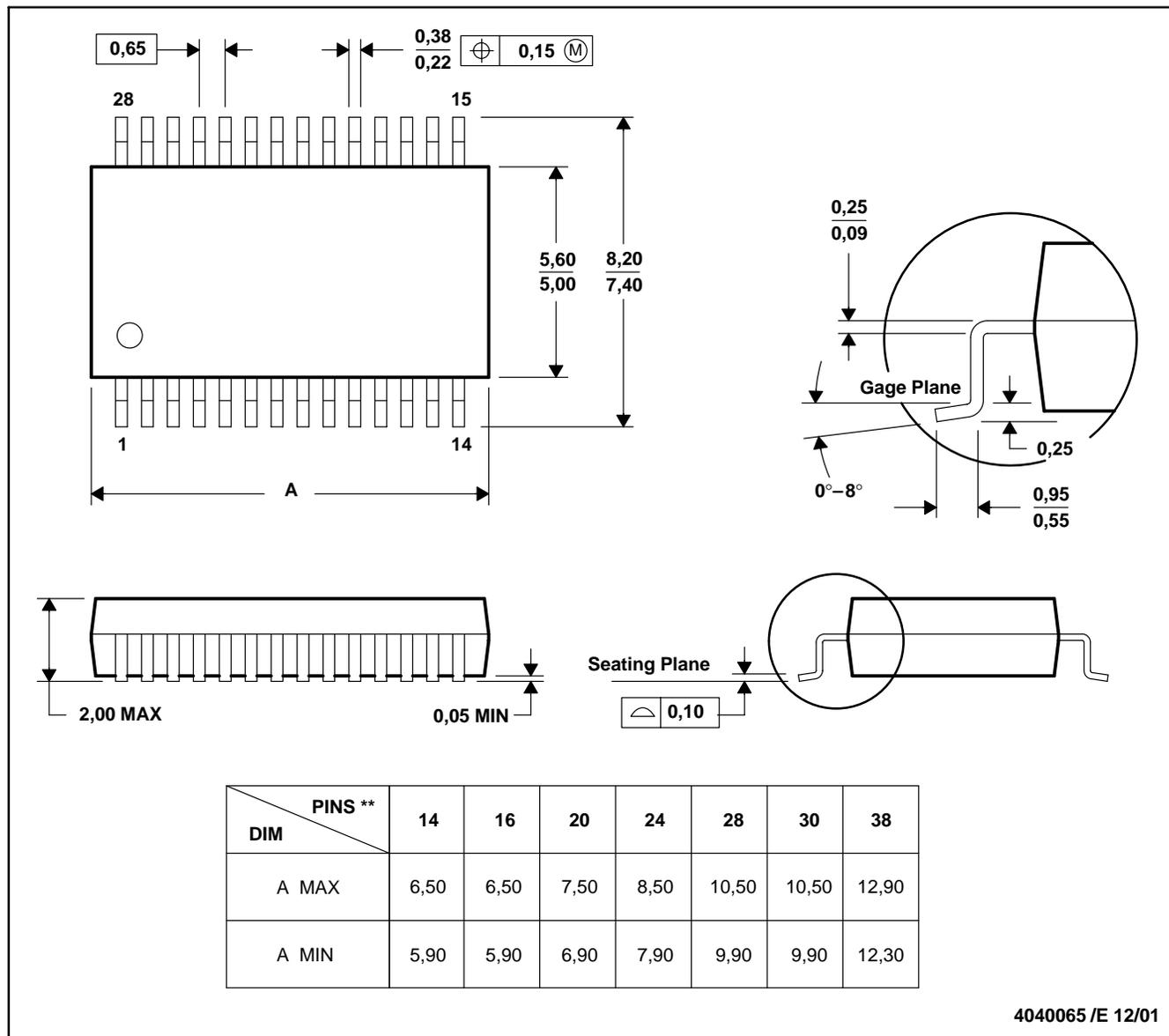
	PINS **	14	16	20	24	28	30	38
DIM								
A MAX		6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN		5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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